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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/076,625	02/19/2002	Atsushi Sakai	50006-138	9551

7590 11/14/2003

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EXAMINER	
ROSS, JOHN M	

ART UNIT	PAPER NUMBER
2188	9

DATE MAILED: 11/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/076,625	SAKAI ET AL.	
	Examiner	Art Unit	
	John M Ross	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *9* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The Information Disclosure Statement(s) received 2 April 2003 has been considered. Please see attached PTO-1449(s).

Drawings

3. The drawings filed on 19 February 2002 have been approved by the Examiner.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Cache Memory System Having Software and Hardware Cache Controllers".

Claim Objections

5. Claims 11 and 12 objected to because of the following informalities: In line 3 of both claims the phrase "the designated address the cache memory" is grammatically incorrect. It is

suggested that the word "of" be inserted after the word "address". The claim(s) will be interpreted in light of this suggestion. Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-6, 9-10, and 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujiwara (Takashi Fujiwara et al, A Custom Processor for the Multiprocessor System ASCA, 1998).

As in claims 1-6, 9-10, and 17-20, Fujiwara describes a cache memory system comprising:

a software cache controller which performs software control for controlling data transfer to the cache memory in accordance with a preliminarily programmed software (Fig.6; section 3.1.3, lines 1-10); and

a hardware cache controller which performs hardware control for controlling data transfer to the cache memory using a predetermined hardware (Section 3.1.3, lines 26-32);

where the processor causes the software cache controller to perform the software control but causes the hardware cache controller to perform the hardware control when it becomes impossible to perform the software control (Section 3.1.3, lines 32-36).

As in claims 2, 4, 6, 10, 18 and 20, Fujiwara describes the above system wherein the processor causes the hardware cache controller to perform hardware control when a cache miss happens at the time of software control (Section 3.1.3, lines 32-36).

As in claims 3-6, Fujiwara describes the above system wherein the software cache controller stores desired data in the cache memory in accordance with a code produced by static prediction of a compiler (Section 3.1.3, lines 8-10).

As in claims 5 and 6, Fujiwara describes the above system wherein before the processor executes a data read-out instruction for reading out desired data of the main memory, the software cache controller reads out data at an address of the main memory designated by the data read-out instruction and stores the data in the cache memory (Section 3.1.3, lines 12-13).

As in claims 9 and 10, Fujiwara describes the above system wherein before the processor executes a data write instruction for writing data in the main memory, the software cache controller designates an address of the cache memory, which is used for storing data from the processor (Section 3.1.3, lines 12-13).

As in claims 17-20, Fujiwara describes the above system wherein the software cache controller is formed by a transfer control processor for controlling data transfer to the cache memory (Fig. 6, element labeled "Data Transfer Controller"; section 3.1.3, lines 6-8).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 7-8 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara (Takashi Fujiwara et al, A Custom Processor for the Multiprocessor System ASCA, 1998) in view of Handy (Jim Handy, The Cache Memory Book, 1998).

Fujiwara is relied upon for the teachings relative to claims 5, 6, 9 and 10 as above.

Fujiwara does not teach that at the same time when the processor executes a data read-out instruction, the software cache controller transfers from the cache memory to the processor the data at the address of the main memory designated by the data read-out instruction, as required by claims 7 and 8.

Fujiwara also does not teach that when the processor executes a data write instruction, the data from the processor written at the designated address of the cache memory is written by the

software cache controller at an address of the main memory designated by the data write instruction, as require by claims 11 and 12.

It is noted that claims 7 and 8 describe a cache read hit, and claims 11 and 12 describe a cache write hit with a write-through policy. Handy teaches that during a cache read hit a cache controller transfers data from the cache memory to the processor (Fig. 2.4a; page 44, paragraph 1). Handy also teaches that during a cache write hit, the cache controller writes data in the cache memory and the main memory (Fig. 2.4c; page 45, paragraph 3). Handy also teaches that using a cache memory greatly increases effective memory speed (Page 204, paragraph 10).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to transfer data from the cache memory to the processor during a cache read hit and to write data in the cache memory and the main memory during a cache write hit as taught by Handy, in the system of Fujiwara, in order to increase effective memory speed through the use of a cache memory as taught by Handy.

10. Claims 13-16 and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara (Takashi Fujiwara et al, A Custom Processor for the Multiprocessor System ASCA, 1998) in view of Hallnor (Erik G. Hallnor et al, A Fully Associative Software-Managed Cache Design, 2000).

Fujiwara is relied upon for the teachings relative to claims 1-4 as above.

The rationale derived from Fujiwara in the rejection of claims 17-20 above is incorporated herein for the teaching that the software cache controller is formed by a transfer control processor for controlling data transfer to the cache memory.

Fujiwara does not teach that the hardware cache controller performs line management of the cache memory by using a multi-way set-associative method and that the software cache controller performs line management of the cache memory by using a fully-associative method for at least one way in the multiple ways, as required by claims 13-16.

It would have been well known to one of ordinary skill in the art at the time of invention by applicant that a cache line management policy may be multi-way set-associative or fully-associative. Hallnor teaches that hardware controlled management is better suited for a low-associativity cache (i.e. multi-way set-associative) due to the reduced complexity compared to a fully-associative cache, and software controlled management is better for fully-associative caches due to the ability to apply sophisticated replacement algorithms (Section 2, paragraphs 1, 3 and 4).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to perform hardware controlled line management of the cache memory by using a multi-way set-associative method, and to perform software controlled line management of the cache memory by using a fully-associative method as taught by Hallnor, in the system of

Fujiwara, according to the teaching of Hallnor that the reduced complexity of a multi-way set-associative cache is better suited to hardware control, and to take advantage of the ability to apply sophisticated replacement algorithms to a software-managed fully-associative cache.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M Ross whose telephone number is (703) 305-0706. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

JMR

Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER